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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,809	09/19/2003	Sridhar Kumar	010327-007810US	6629
20350 7590 06/21/2007 TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			EXAMINER HOANG, HIEU T	
			ART UNIT 2152	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/665,809

Applicant(s)

KUMAR ET AL.

Examiner

Hieu T. Hoang

Art Unit

2152

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the communication filed on 09/19/2003.
2. Claims 1-16 are pending and presented for examination.

Specification

3. The disclosure is objected to because of the following informalities.
4. The specification recites, on p. 4 lines 1-2, "data received at access equipment systems 6 are then sent to routers 8" according to fig. 1. However, there are no "routers 8" shown in fig. 1. Appropriate correction is required.
5. The specification recites, on p. 5 lines 2-3, "data maybe transferred from a port 208 in one data processor 201 to a port 208 in the same data processor 201 or a different data processor 201." It is not clearly understood whether the two ports on the same data processor are the same port or different. For examining purpose, the second port on the same data processor will be treated as "another port." Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5-8, 11, 12, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith (US 5,561,768).

8. For claim 1, Smith discloses a telecommunications device for processing data, wherein the device includes a plurality of data processors, the device comprising:

- a plurality of control processors, each control processor configured to manage data routing paths for routing data between data processors in the plurality of data processors (col. 3 lines 50-59, col. 4 lines 59-67, each control processor receives communications from and transmits communications to one or more processing nodes); and
- a plurality of logical nodes, wherein each logical node includes one or more data processors in the telecommunications device and is associated with a control processor in the plurality of control processor (col. 3 lines 50-59, each logical partition is read as a logical node including plurality of processing nodes or data processors, each logical partition is controlled by a control processor), wherein a logical node routes data using the one or more data processors included in the logical node according to the data routing paths for routing data associated with each logical data processor (fig. 3A, col. 3 lines 50-59, col. 4 lines 59-67, each control processor routes data communications among processing nodes

associated with the logical partition).

9. For claim 6, Smith discloses a telecommunications shelf including a plurality of slots configured to connect to data processors, the shelf comprising:

- a first logical shelf including a first set of one or more data processors, wherein each data processor in the first set is connected to a first set of one or more slots in the plurality of slots; and a second logical shelf including a second set of one or more data processors, wherein each data processor in the second set is connected to a second set of one or more slots in the plurality of slots (col. 3 lines 50-59, col. 4 lines 59-67, fig. 3A, each logical shelf is a logical partition comprising a control processor controlling data processing for a plurality of processors, each processor is attached to a slot in the array of processors, there can be more than two logical partitions or logical shelves),
- wherein the first logical shelf is associated with a first entity that transfers data using the first set of one or more data processors and second logical shelf is associated with a second entity that transfers data using the second set of one or more data processors (lines 50-59, col. 4 lines 59-67, each entity is read as a separate application run on each logical partition).

10. For claim 12, Smith discloses a method for routing data using a telecommunications device that includes a plurality of data processors, the method comprising:

- configuring a first set of one or more data processors in the plurality of data processors for a first logical node in the telecommunications device; configuring a second set of one or more data processors in the plurality of data processors for a second logical node in the telecommunications device (col. 3 lines 50-59, col. 4 lines 59-67, fig. 3A, each logical node is a logical partition comprising a control processor providing data processing for a plurality of processors, there can be more than two logical partitions);
- receiving data associated with a first entity; routing the data using the one or more data processors in the first logical node; receiving data associated with a second entity; and routing the data using the one or more data processors in the second logical node (col. 3 lines 50-59, col. 4 lines 59-67, fig. 3A, a control processor processes data routing for a plurality of processors within that logical partition).

11. For claim 2, Smith further discloses a power source configured to power the plurality of logical nodes (fig. 1, since there is a system clock for the whole system of logical nodes and array of processors that consume power, it is inherent there has to be a power source for these logical nodes, besides a power source to power the system inherently exists in communications system and is known in the art, also see, Van Doren, [0056] for power system).

12. For claim 3, Smith further discloses a plurality of physical slots, wherein each of the plurality of data processors are coupled to a physical slot in the plurality of physical slots (fig. 3A, each processor located at the leaf is associated with a physical slot in the processor array).

13. For claim 5, Smith further discloses each control processor and its associated logical node is configured to transfer data for a separate entity (col. 3 lines 50-59, each logical node can be used to process a single application, read as an entity).

14. For claim 7, Smith further discloses a first control processor associated with the first logical shelf; and a second control processor associated with the second logical shelf (col. 3 lines 50-59, col. 4 lines 59-67, a logical shelf can be read as a shelf of processors that belong to a logical partition; each control processor receives communications from and transmits communications to one or more processing nodes).

15. For claim 8, Smith further discloses the first control processor is configured to manage data routing paths for the first entity and the second control processor is configured to manage data routing paths for the second entity (col. 3 lines 50-59, each logical node can be used to process a single application, read as an entity).

16. For claim 11, Smith further discloses comprising a power source configured to provide power to the first and second set of one or more data planes in the first and second logical shelves (same rationale as in claim 2).

17. For claim 15, Smith further discloses configuring a first control processor associated with the first logical node; and configuring a second control processor associated with the second logical node (col. 3 lines 50-59, col. 4 lines 59-67, each control processor receives communications from and transmits communications to one or more processing nodes).

18. For claim 16, the claim is rejected for the same rationale as in claim 5.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. For claim 10, the claim is rejected for the same rationale as in claim 9.

24. For claim 13, Smith further discloses receiving data associated with the first entity comprises receiving data for a first routing data path from a first location to a second location in the telecommunications device, and further comprising determining a third and fourth location in the telecommunications device in which to route the received data, wherein routing the data comprises routing the data from a data processor in the third location to a data processor in the fourth location, the third and fourth data processors included in the first set of data processors (Van Doren, [0047], a address mapping technique that uses logical ID of a logical partition QBB to translate starting address to physical location of a certain processor, for instance, mapping the first entity's first location to the third location and the first entity's second location to the fourth location, wherein the third and fourth locations are in one logical partition specifically for that entity).

25. For claim 14, the claim is rejected for the same rationale as in claim 13.

20. Claims 4, 9, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith as applied to claim 3, 6 and 12 above, and further in view of Van Doren (US 2001/0037435).

21. For claim 4, Smith discloses the invention as in claim 3. Smith does not disclose a data path from a first physical slot location to a second physical slot location in the device is mapped to a third physical slot location to a fourth physical slot location.

However, Van Doren discloses the same (fig. 5, [0007], [0011], [0013], a multiprocessor system that has common address space for multiple partitions, each comprising processors, routing messages are associated with a routing context which is looked up in a routing table to determine which physical connection or location the corresponding processor can be found)

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Smith and Van Doren to provide an efficient means for flexible configuration and partitioning in a multiprocessor computing system (Van Doren, [0010])

22. For claim 9, the claim is rejected fro the same rationale as in claim 4. Smith-Van Doren further discloses the first control processor is configured to map data routing paths based on a location of the first set of slots in the telecommunications shelf (Van Doren, [0047], a address mapping technique that uses logical ID of a logical partition QBB to translate starting address to physical location of a certain processor).

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Beukema et al. US 7,149,220. Data transfer.
- Denneau et al. US 5,566,342. Scalable switch wiring for large arrays of processors.
- Gilbert. US 2004/0123035. Tag entries.
- Hyytiainen. US 2005/0147027. Hub for loop initialization.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu T. Hoang whose telephone number is 571-270-1253. The examiner can normally be reached on Monday-Thursday, 8 a.m.-5 p.m., EST.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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